REMARKS

Introduction

Applicants note with appreciation the Examiner's indication that references cited in the Information Disclosure Statement of March 25, 2004 have been considered.

Upon entry of the foregoing amendment, claims 1-27 are pending in the application. Claims 1, 3, 12, 14, and 15 have been amended. New claims 17-27 have been added. No new matter is being presented. In view of the following remarks, reconsideration and allowance of all the pending claims are requested.

Claim Objections

Claim 15 has been objected to as containing minor informalities. Applicants have amended claim 15 to correct these informalities. Accordingly, Applicants' respectfully request that the Examiner withdraw the objection.

Rejection under 35 USC §102 based on Alves et al.

Claims 1-6 and 11-16 have been rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent Application Publication No. 2003/0007636 to Alves et al. Applicants respectfully request reconsideration of these claims for at least the following reasons.

Claims 1-6

At page 3 of the Office Action of June 7, 2006, the Examiner relies on FIG. 2 of Alves et al. and "the first 3 RCs, each RC has n registers, see figure 3, 312" as "first, second, and third memory devices," as recited in Applicants' independent claim 1. In addition, the Examiner relies on FIG. 2 of Alves et al. and "the first three RCs in the second row, each cell has a calculation circuit and memory circuit" as being equivalent to Applicants' "fourth memory device, calculation element, and fifth memory device," as recited in independent claim 1 of Applicants' invention.

Finally, the Examiner relies on "the third row" of RCs shown in FIG. 2 of Alves et al. as being the same as Applicants' "sixth, seventh, and eight memory devices," as recited in independent claim 1. Thus, it is apparent that the Examiner is relying on each of the RCs shown in FIG. 2 of Alves et al. as being either "a memory device" or "a calculation element" in an effort to allegedly meet the combination presently recited in Applicants' independent claim 1.

However, contrary to the Examiner's interpretation, the second RC in the second row shown in FIG. 2 of Alves et al. cannot be interpreted as "the calculation element ... surrounded by the first through the eight memory devices and ... directly connected with each of the first through the eight memory devices," since this RC (which the Examiner relies on as "the calculation element") is not "directly connected with each of the first through eight memory devices," as presently recited by independent claim 1 of Applicants' invention. In contrast with the present invention, the second RC in the second row shown in FIG. 2 of Alves et al. is only directly connected with **four other RCs** (i.e., the second RC in the first row, the first RC in the second row, the third RC in the second row, and the second RC in the third row). Accordingly, Applicants respectfully submit that the arrangement shown in Alves et al. FIG. 2 does not include a "calculation element ... surrounded by the first through the eight memory devices and ... directly connected with each of the first through the eight memory devices," as presently recited in independent claim 1 of Applicants' invention.

Similarly, regarding the Examiner's assertion that the registers 312 can read as Applicants' "memory devices," it is clear from FIG. 3 of Alves et al. that the registers 312 being relied on by the Examiner are not "directly connected with" any of the surrounding RCs. In contrast with the present invention, these registers 312 are directly connected with components that are all within **the same RC**. For example, these registers 312 are directly connected with an output mux 318, an AND gate 303, and a shifter 306 within the respective RC. Since these are the only elements with which the registers 312 are "directly connected," the registers 312 shown in FIG. 3 of Alves et al. cannot be interpreted as Applicants' "first through eight memory devices...directly connected with [the calculation element]," as presently recited in independent claim 1.

For the reasons set forth above, it is respectfully submitted that Alves et al. fails to

disclose, among other things, "the calculation element is surrounded by the first through the eight memory devices and is directly connected with each of the first through the eight memory devices," as presently recited in independent claim 1 of Applicants' invention.

"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as contained in the...claim." Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). "The elements must be arranged as required by the claim..." In re Bond, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990). Further, in the event that the Office Action is relying on the theory of inherency in any manner, "the Examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied art." *Ex parte Levy*, 17 USPQ2d 1461, 1464 (Bd. Pat. App. & Inter. 1990) (emphasis in original). See also MPEP 2112. Accordingly, since Alves et al. does not explicitly or inherently teach every element as presently recited in independent claim 1, Alves et al. cannot be properly used to reject independent claim 1 under 35 U.S.C. § 102. Therefore, it is respectfully submitted that independent claim 1 is allowable over Alves et al., and withdrawal of this rejection is earnestly solicited.

Regarding claims 2-6, it is respectfully submitted that for at least the reasons that each of claims 2-6 depends from independent claim 1, and therefore contain each of the features as presently recited in this claim, claims 2-6 are therefore also patentable over Alves et al. Accordingly, withdrawal of the rejection of these claims is also earnestly solicited.

Claim 11

At page 3 of the Office Action of June 7, 2006, the Examiner relies on "the first 3 RCs, each RC has n registers, see figure 3, 312" as being "first, second, and third memory devices," as recited Applicants' independent claim 11. In addition, the Examiner relies on a row decoder 220 shown in FIG. 2 of Alves et al. as being equivalent to Applicants' "first communication port," as recited in independent claim 11 of Applicants' invention.

However, Alves et al., at page 2, paragraph [0016], describes that the row decoder 220 addresses and instructs all RC's 200 in each row of array in FIG. 2 such that a row address signal from the row decoder 220 is gated with the column address signal from the column decoder 230 at each RC 200 to activate and instruct a selected one or more of the RCs 200 in the array. Furthermore, Alves et al., at page 2, paragraph [0020], describes that a storage register 312 temporarily stores functional unit comparison results in the RCs.

Thus, it is clear from this description in Alves et al. that the row decoder 220 merely provides the row address signal that is gated with the column address signal in order to select RCs 200 in the array. It is also clear that this row address signal received via the row decoder 220 is not then stored by the RCs 200, as apparently alleged by the Examiner. Rather, as pointed out by Alves et al. in paragraph [0020] the storage registers 312, being relied on by the Examiner as the "memory devices," only store data generated within the RCs 200 (i.e., the functional unit comparison results from 310, 320, and 330). Since it is evident that these storage registers 312 do not store the row address signal, the Examiner's interpretation of Alves et al. cannot be supported.

Thus, Alves et al.'s row decoder 220 is not the same as Applicants' "first communication port" and Alves et al.'s "storage registers 312" are not the same as Applicants' "first, second, and third memory devices." Since (1) Alves et al.'s row address signal cannot be interpreted as "data received [and stored] in first, second, and third memory devices" and (2) the storage registers 312 of Alves et al. do not store "data received through a first communication port," Alves et al. fails to disclose, among other things, "storing data received through a first communication port in first, second, and third memory devices arranged in a first row direction of the DSP architecture, or in sixth, seventh, and eighth memory devices arranged in a third row direction of the DSP architecture," as recited in independent claim 11 of Applicants' invention.

For at least the same reasons, Alves et al. fails to disclose, among other things, "storing data received through *a second communication port* in the first and the sixth memory devices and a fourth memory device that are arranged in a first column direction of the DSP architecture, or in the third and the eighth memory devices and a fifth memory device that are arranged in a third column direction of the DSP architecture," also as recited in independent

claim 11 of Applicants' invention.

Finally, Applicants respectfully submit that at no point does Alves et al. disclose "processing the data stored in the first through the eighth memory devices, using a calculation element disposed between the fourth and the fifth memory devices arranged in a second row direction of the DSP architecture and between the second and the seventh memory devices arranged in a second column direction of the DSP architecture," as recited in independent claim 11 of Applicants' invention. In other words, contrary to what the Examiner's interpretation would require from Alves et al. for support, at no point does Alves et al. disclose or even mention that the second RC 200 in the second row "process[ing] the data stored in" (1) each of the first, second, and third RCs 200 in the first row of the array of FIG. 2, (2) each of the first and third RCs 200 in the second row of the array of FIG. 2, and (3) each the first, second, and third RCs in the third row of the array of FIG. 2. Accordingly, Applicants respectfully submit that Alves et al. fails to disclose, among other things, "processing the data stored in the first through the eighth memory devices, using a calculation element disposed between the fourth and the fifth memory devices arranged in a second row direction of the DSP architecture and between the second and the seventh memory devices arranged in a second column direction of the DSP architecture," as recited in independent claim 11 of Applicants' invention.

Accordingly, since Alves et al. does not explicitly or inherently teach every element as presently recited in independent claim 11, Alves et al. cannot be properly used to reject independent claim 11 under 35 U.S.C. § 102. Therefore, it is respectfully submitted that independent claim 11 is allowable over Alves et al., and withdrawal of this rejection is earnestly solicited.

Claims 12 and 13

For at least the reasons set forth above with respect to independent claims 1 and 11, it is respectfully submitted that Alves et al. also fails to disclose, among other things, "a first communication port to receive data... at least three memory devices connected with the first communication port ... to temporarily store at least a first portion of the data received at the first communication port... a calculation element connected with each of the memory devices of the first, second and third rows of the DSP architecture to process and transfer the first and second

portions of the data temporarily stored in the at least three memory devices in the first and third rows," as presently recited in independent claim 12 of Applicants' invention.

Accordingly, since Alves et al. does not explicitly or inherently teach every element as presently recited in independent claim 14, Alves et al. cannot be properly used to reject independent claim 14 under 35 U.S.C. § 102. Therefore, it is respectfully submitted that independent claim 14 is allowable over Alves et al., and withdrawal of this rejection is earnestly solicited.

Regarding claim 13, it is respectfully submitted that for at least the reason that claim 13 depends from independent claim 12, and therefore contains each of the features as presently recited in this claim, claim 13 is therefore also patentable over Alves et al. Accordingly, withdrawal of the rejection of this claim is also earnestly solicited.

Claims 14-16

With reference to independent claim 14, Applicants first respectfully note that the Examiner has not addressed the feature of "a second communication port," as originally recited in Applicants' independent claim 14. Accordingly, the Examiner has not shown that Alves et al. anticipates independent claim 14.

Furthermore, Alves et al. is directed to a method and apparatus for executing a block cipher routine using a reconfigurable data path array. *See* Alves et al. page 1, paragraph [0001]. More particularly, Alves et al. describes a data processing architecture shown in FIG. 1 as including a processing engine 102, a software programmable core processor 104, and a reconfigurable array of processing elements 106 that each perform a specific function. *See* Alves et al. page 1, paragraph [0010]. The array of reconfigurable RCs 200 has a row decoder 220 and a column decoder 230 to receive a row address signal and a column address signal, respectively, to select certain ones of the RCs 200. *See* Alves et al. FIG. 2.

The Examiner relies on the row decoder 220 shown in FIG. 2 of Alves et al. to allegedly read as Applicants' "first communication port." However, it is clear from FIG. 2 and the description in Alves et al. that the row decoder 220 does not receive "first motion picture image data divided into image frames," as presently recited in independent claim 14 of Applicants' invention. In contrast with the present invention, Alves et al.'s row decoder 220 receives the

row address signal, which is a mere selection signal, and therefore is not a data signal. Since Alves et al.'s row decoder 220 does not receive ,"motion picture image data," Alves et al.'s row decoder 220 is not the same as Applicants' "first communication port," as presently recited in independent claim 14.

Additionally, Alves et al. does not even relate to "motion picture image data divided into image frames," as presently recited in independent claim 14 of Applicants' invention. Thus, Alves et al. fails to disclose, among other things, "a first communication port to receive first motion picture image data divided into image frames" and "a second communication port to receive second motion picture image data divided into image frames," as presently recited in independent claim 14 of Applicants' invention.

Furthermore, the Examiner relies on the storage registers 312 of the RCs 200 shown in FIG. 3 of Alves et al. as allegedly being equivalent to Applicants' "first through eight memories." However, these storage registers 312 do not "store respective ones of the image frames of the first and second motion picture image data," as presently recited in independent claim 14 of Applicants' invention. Accordingly, Alves et al. also fails to disclose, among other things, "first through eight memories to store respective ones of the image frames of the first and second moving image data," as presently recited in independent claim 14.

Accordingly, since Alves et al. does not explicitly or inherently teach every element as presently recited in independent claim 14, Alves et al. cannot be properly used to reject independent claim 14 under 35 U.S.C. § 102. Therefore, it is respectfully submitted that independent claim 14 is allowable over Alves et al., and withdrawal of this rejection is earnestly solicited.

Regarding claims 15 and 16, it is respectfully submitted that for at least the reasons that each of claims 15 and 16 depends from independent claim 14, and therefore contain each of the features as presently recited in this claim, claims 15 and 16 are therefore also patentable over Alves et al. Accordingly, withdrawal of the rejection of these claims is also earnestly solicited.

Rejection under 35 USC §102 based on Sasaki et al.

Claims 1-6 and 11-16 are rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent Application Publication No. 2003/0330562 to Sasaki et al. Applicants respectfully request reconsideration of this rejection for at least the following reasons.

Claims 1-6

Applicants first respectfully point out that the Examiner has not addressed the feature of "a first communication port," as recited in independent claim 1 of Applicants' invention. Furthermore, FIG. 14 of Sasaki et al. on which the Examiner relies does not show "a first communication port...connected with [first, second, and third memory devices; and sixth, seventh, and eighth memory devices]." Nor is this feature inherently disclosed in Sasaki et al. Accordingly, Applicants respectfully submit that Sasaki et al. does not anticipate each feature of independent claim 1.

Furthermore, the Examiner apparently relies on a matrix of processing elements PE shown in FIG. 14 of Sasaki et al., as allegedly reading on both the "memory devices" and the "calculation element," as recited in independent claim 1 of Applicants' invention. *See* Office Action of June 7, 2006 page 3, item 7. In particular, the Examiner relies on local memories of processing elements PEs of a completely different embodiment shown in FIG. 18 of Sasaki et al. as Applicants' "memory devices."

Applicants submit that the embodiment of FIG. 14 of Sasaki et al. and the embodiment of FIG. 18 of Sasaki et al. are entirely different from one another. Such a reliance on a combination of different embodiments in order to attempt to meet the requirements of an anticipation rejection of Applicants' claims is improper. "An invention is anticipated if the same device, including all the claim limitations, is shown in a single prior art reference. Every element of the claimed invention must be literally present, arranged as in the claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9USPQ2d 1913, 1920 (Fed Cir. 1989). Moreover, FIG. 14 is the admitted prior art of Sasaki et al. and does not even illustrate use of the local memories 1043-1, 1043-2, etc. of FIG. 18, as it shouldn't since the embodiments of FIGS. 14 and 18 are different devices that perform different operations. More specifically, the

embodiment illustrated in FIG. 14 of Sasaki et al., which is described at paragraph [0012] of the "BACKGROUND OF THE INVENTION" section is directed to a conventional multi-processor unit having processor elements (PEs) arranged in a matrix, but no "memory devices." *See* Sasaki et al. paragraph [0012] and FIG. 14. In contrast, the embodiment illustrated in FIG. 18 of Sasaki et al., which is described at paragraphs [0104] and [0105], is directed to a processor element board 1031-1 of the invention having child and parent processor elements with local memories, but does not include the structure of the prior art embodiment of FIG. 14 in Sasaki et al. In fact, the embodiment of FIG. 18 of Sasaki et al. shows a tree structure that is completely different from the matrix structure of the prior art embodiment of FIG. 14, therefore, it is evident that these embodiments necessarily operate differently. Since the Examiner relies on an improper combination of different embodiments in an effort to meet each of the elements presently recited in independent claim 1, the Examiner's §102(b) rejection is improper, and should be withdrawn.

Furthermore, it is respectfully submitted that neither one of the embodiments of FIGS. 14 and 18 of Sasaki et al. alone discloses the features presently recited in independent claim 1 of Applicants' invention, namely, "first, second, and third memory devices... arranged in a first row direction of the DSP architecture," "a fourth memory device, a calculation element, and a fifth memory device... in a second row direction below the first row direction of the DSP architecture," and "sixth, seventh, and eighth memory devices... arranged in a third row direction of the DSP architecture, wherein the calculation element is surrounded by the first through the eight memory devices and is directly connected with each of the first through the eight memory devices."

Finally, even if the Examiner's combination of two entirely different embodiments were proper (which it is not), none of the PE's shown in FIG. 18 of Sasaki et al. are "directly connected with [surrounding memory devices]," as presently recited in independent claim 1 of Applicants' invention. In contrast with the present invention, Sasaki et al. describes these memories 1043-1, etc. as being "local memories...built therein." *See* Sasaki et al. paragraph [0105]. Thus, it is evident from this description in Sasaki et al. that a PE must first access a neighboring PE, and, in turn, the neighboring PE accesses its own local built in memory. In other words, none of the PE's shown in FIG. 18 of Sasaki et al. is "directly connected with" the

local memory of a neighboring PE. Accordingly, none of Sasaki et al.'s PE's can be interpreted as being the same as Applicants' "the calculation element ... directly connected with each of the first through the eight memory devices." Therefore, Sasaki et al. fails to disclose this feature, as presently recited in independent claim 1 of Applicants' invention.

Accordingly, since Sasaki et al. does not explicitly or inherently teach every element as presently recited in independent claim 1, Sasaki et al. cannot be properly used to reject independent claim 1 under 35 U.S.C. § 102. Therefore, it is respectfully submitted that independent claim 1 is allowable over Sasaki et al., and withdrawal of this rejection is earnestly solicited.

Regarding claims 2-6, it is respectfully submitted that for at least the reasons that each of claims 2-6 depends from allowable independent claim 1, and therefore contain each of the features as presently recited in this claim, claims 2-6 are therefore also patentable over Sasaki et al. Accordingly, withdrawal of the rejection and allowance of these claims is also earnestly solicited.

Claim 11

Applicants first respectfully point out that the Examiner has not addressed the feature of "a first communication port," as recited in independent claim 11 of Applicants' invention. Accordingly, the Examiner has not shown that Sasaki et al. anticipates each feature of independent claim 11.

Furthermore, at no point does Sasaki et al. disclose "processing the data stored in the first through the eighth memory devices, using a calculation element disposed between the fourth and the fifth memory devices arranged in a second row direction of the DSP architecture and between the second and the seventh memory devices arranged in a second column direction of the DSP architecture," as recited in independent claim 11.

In contrast with the present invention, Sasaki et al. describes, at page 2, paragraphs [0014] and [0015], that each of the processor elements 1001 (PEs) of FIG. 14 performs an arithmetic operation on corresponding ones of the blocks of volume data BK000, BK010, etc. shown in FIG. 15. Sasaki et al. further describes in paragraph [0014] that since the arithmetic

operation is distributed in accordance with a single distribution method, suitable amounts of arithmetic operation are not sometimes distributed. Thus, it is evident from this description that none of Sasaki et al.'s PE's processes data stored in other surrounding PE's, as apparently alleged by the Examiner. Instead, each one of the processing elements PEs only processes one block of volume data (FIG. 15), and further Sasaki et al. does not disclose anything about volume data being stored in one PE and being accessed and processed by another PE. Accordingly, Sasaki et al. fails to disclose "processing the data stored in the first through the eighth memory devices, using a calculation element disposed between the fourth and the fifth memory devices arranged in a second row direction of the DSP architecture and between the second and the seventh memory devices arranged in a second column direction of the DSP architecture," as presently recited in independent claim 11 of Applicants' invention.

In fact, the Examiner apparently relies on a combination of the PEs shown in FIG. 14 of the prior art section of Sasaki et al. with the PE's shown in FIG. 18 of Sasaki et al.'s detailed description. However, it can be seen from a comparison of these two figures and their respective descriptions that these two embodiments are entirely different from each other. Furthermore, the Examiner has not provided any evidence of how these two entirely different embodiments can be combined to meet the explicit recitations of independent claim 11. Applicants respectfully submit that neither one of these embodiments, nor any hypothetical combination thereof, disclose "processing the data stored in the first through the eighth memory devices, using a calculation element disposed between the fourth and the fifth memory devices arranged in a second row direction of the DSP architecture and between the second and the seventh memory devices arranged in a second column direction of the DSP architecture," as recited in independent claim 11 of Applicants' invention.

Accordingly, since Sasaki et al. does not explicitly or inherently teach every element as recited in independent claim 11, Sasaki et al. cannot be properly used to reject independent claim 11 under 35 U.S.C. § 102. Therefore, it is respectfully submitted that independent claim 11 is allowable over Sasaki et al., and withdrawal of this rejection is earnestly solicited.

Claims 12 and 13

Applicants again respectfully point out that the Examiner has not addressed the feature

of "a first communication port," as recited in independent claim 12 of Applicants' invention. Accordingly, the Examiner has not shown that Sasaki et al. anticipates each feature of independent claim 12.

Furthermore, at no point does Sasaki et al. disclose "at least three memory devices ... to temporarily store at least a first portion of the data received at the first communication port ...at least three memory devices... to temporarily store at least a second portion of the data received at the first communication port... and a calculation element connected with each of the memory devices of the first, second and third rows of the DSP architecture to process and transfer the first and second portions of the data temporarily stored in the at least three memory devices in the first and third rows," as presently recited in independent claim 12 of Applicants' invention.

In contrast with the present invention, Sasaki et al. describes, at page 2, paragraphs [0014] and [0015], that each of the processor elements 1001 (PEs) of FIG. 14 performs an arithmetic operation on corresponding ones of the blocks of volume data BK000, BK010, etc. shown in FIG. 15. Sasaki et al. further describes in paragraph [0014] that since the arithmetic operation is distributed in accordance with a single distribution method, suitable amounts of arithmetic operation are not sometimes distributed. Thus, it is clear from this description that none of Sasaki et al.'s PE's processes data stored in other surrounding PE's. Instead, each one of the processing elements PEs only processes one block of volume data (FIG. 15), and further Sasaki et al. does not disclose anything about volume data being stored in one PE and being transferred and processed by another PE. Accordingly, Sasaki et al. fails to disclose "a calculation element connected with each of the memory devices of the first, second and third rows of the DSP architecture to process and transfer the first and second portions of the data temporarily stored in the at least three memory devices in the first and third rows," as presently recited in independent claim 12 of Applicants' invention.

In fact, the Examiner apparently relies on a combination of the PEs shown in FIG. 14 of the prior art section of Sasaki et al. with the PE's shown in FIG. 18 of Sasaki et al.'s detailed description. However, it can be seen from a comparison of these two figures and their respective descriptions that these two embodiments are entirely different from each other. Furthermore, the Examiner has not provided any evidence of how these two entirely different

embodiments can be combined to meet the explicit recitations of independent claim 12. Applicants respectfully submit that neither one of these embodiments, nor a combination thereof, disclose "at least three memory devices ... to temporarily store at least a first portion of the data received at the first communication port ...at least three memory devices... to temporarily store at least a second portion of the data received at the first communication port... and a calculation element connected with each of the memory devices of the first, second and third rows of the DSP architecture to process and transfer the first and second portions of the data temporarily stored in the at least three memory devices in the first and third rows," as presently recited in independent claim 12 of Applicants' invention.

Accordingly, since Sasaki et al. does not explicitly or inherently teach every element as presently recited in independent claim 12, Sasaki et al. cannot be properly used to reject independent claim 12 under 35 U.S.C. § 102. Therefore, it is respectfully submitted that independent claim 12 is allowable over Sasaki et al., and withdrawal of this rejection and allowance of this claim is earnestly solicited.

Regarding claim 13, it is respectfully submitted that for at least the reason that claim 13 depends from allowable independent claim 12, and therefore contains each of the features as presently recited in this claim, claim 13 is therefore also patentable over Sasaki et al. Accordingly, withdrawal of the rejection and allowance of this claim is also earnestly solicited.

Claims 14-16

Applicants again respectfully point out that the Examiner has not addressed the feature of "a first communication port" and "a second communication port," as recited in independent claim 14 of Applicants' invention. Accordingly, the Examiner has not shown that Sasaki et al. anticipates each features of independent claim 14.

Furthermore, Sasaki et al. is directed to an image processing apparatus and method suitable for use to produce sectional image data of a specimen based on projection image data acquired using, for example, an X-ray single scan cone bean. *See* Sasaki et al. paragraph [0001]. More particularly, Sasaki et al. deals with performing arithmetic operations regarding a volume rendering process using processing elements to perform the operations on volume data

obtained from sectional image data of the X-ray device. *See* Sasaki et al. paragraph [0017]. Thus, Sasaki et al. is limited to sectional X-ray image data, and does not disclose processing motion picture image data in image frames. In fact, Sasaki et al. does not mention anything about "motion picture image data" processing, as presently recited in independent claim 14 of Applicants' invention. Furthermore, Sasaki et al.'s processing elements PEs, being relied on by the Examiner, do not "store respective...image frames," as presently recited in independent claim 14 of Applicants' invention. Accordingly, Applicants respectfully submit that Sasaki et al. fails to disclose, among other things, "first through eight memories to store respective ones of the image frames of the first and second motion picture image data," as presently recited in independent claim 14 of Applicants' invention.

In addition, for similar reasons set forth above with respect to independent claim 11 of Applicants' invention, none of the processing elements PE shown in either FIG. 14 or FIG. 18 of Sasaki et al. can properly be interpreted as being "a calculation element to access the respective image frames of the first through eight memories," as presently recited in independent claim 14 of Applicants' invention. In other words, each of the processor elements 1001 (PEs) of FIG. 14 performs an arithmetic operation on corresponding ones of the blocks of volume data BK000, BK010, etc. shown in FIG. 15, and none of Sasaki et al.'s PEs processes data stored in other surrounding PE's. Instead, each one of the processing elements PEs only processes one block of volume data (FIG. 15), and further Sasaki et al. does not disclose anything about volume data being stored in one PE and being accessed by another PE. Accordingly, Sasaki et al. fails to disclose "a calculation element to access the respective image frames of the first through eight memories," as presently recited in independent claim 14 of Applicants' invention.

Accordingly, since Sasaki et al. does not explicitly or inherently teach every element as presently recited in independent claim 14, Sasaki et al. cannot be properly used to reject independent claim 14 under 35 U.S.C. § 102. Therefore, it is respectfully submitted that independent claim 14 is allowable over Sasaki et al., and withdrawal of this rejection and allowance is earnestly solicited.

Regarding claims 15 and 16, it is respectfully submitted that for at least the reasons that

each of claims 15 and 16 depends from allowable independent claim 14, and therefore contain each of the features as presently recited in this claim, claims 15 and 16 are therefore also patentable over Sasaki et al. Accordingly, withdrawal of the rejection and allowance of these claims is also earnestly solicited.

New Claims

Claims 17-27 have been newly added. New claims 17 and 18 further define features recited in independent claims 11 and 14, respectively. New independent claim 19 recites features, which are not taught in the prior art of record, for example, "a plurality of memories being a first type of device to store image data" and "a plurality of calculation units being a second type of device different from the first type of device and being arranged among the memories and having a plurality of independent connections to adjacent ones of the memories and to access the adjacent memories and process the image data stored therein." New claims 20-23 further define the features recited in independent claim 19. New independent claim 24 also recites features, which are not taught in the prior art of record, for example, "a communication port to receive image data" and "a plurality of image segmentation units arranged in an array to receive the image data from the communication port, each of the image segmentation units including a plurality of memory devices to store portions of the image data and a calculation unit to retrieve and process the stored portions of the image data." New claims 25 and 26 further define features recited in independent claim 24. New independent claim 27 also recites features, which are not taught in the prior art of record, for example, "a plurality of memories being a first type of device to store data," "a plurality of calculation units being a second type of device different from the first type of device and being arranged among the memories having a plurality of connections to directly access adjacent ones of the memories and to process the data stored in the adjacent memories" and "a plurality of communication ports to receive the data and to provide the data to the memories, each communication port being directly connected to at least two memories." Applicants respectfully submit that support for the newly added claims can be found in FIGS. 3, 6, and 7 and corresponding portions of the specification. Accordingly, it is respectfully submitted that new claims 17-27 do not present new

matter, and are allowable over the prior art of record, and allowance of these claims are earnestly solicited.

Conclusion

It is respectfully submitted that a full and complete response has been made to the outstanding Office Action and, as such, there being no other objections or rejections, this application is in condition for allowance, and a notice to this effect is earnestly solicited.

If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at the number provided below.

A $950 fee for additional claims has been incurred by this Amendment. If any further fees are required in connection with the filing of this amendment, please charge the same to out Deposit Account No. 502827.

Respectfully submitted,

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Dated: September 7, 2006

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